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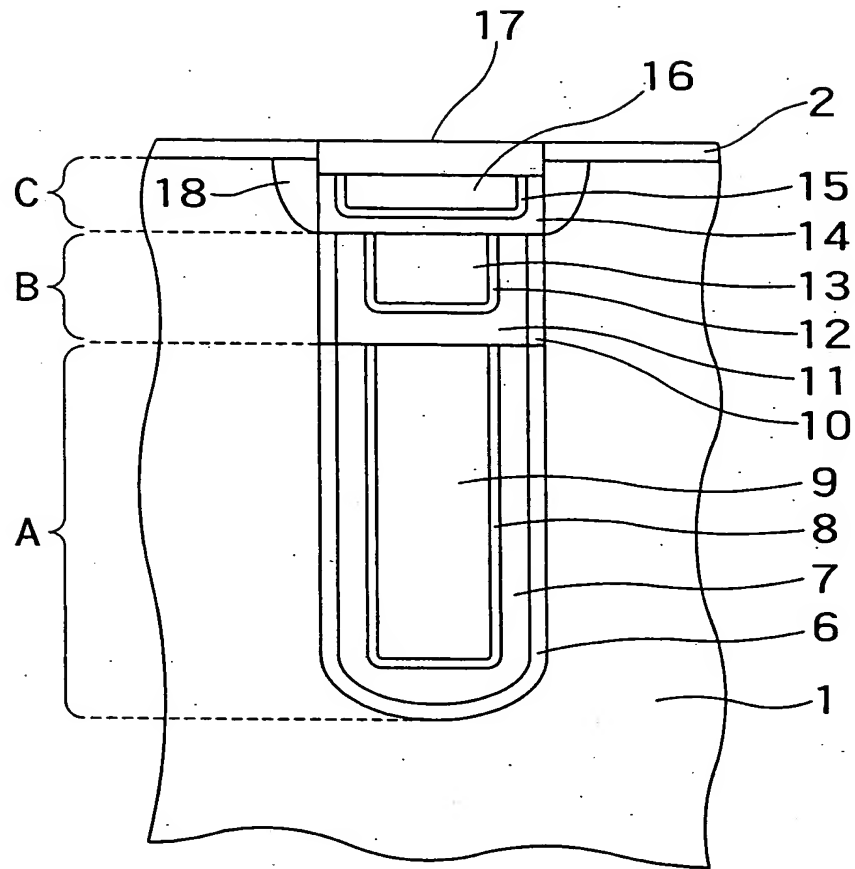


FIG. 1

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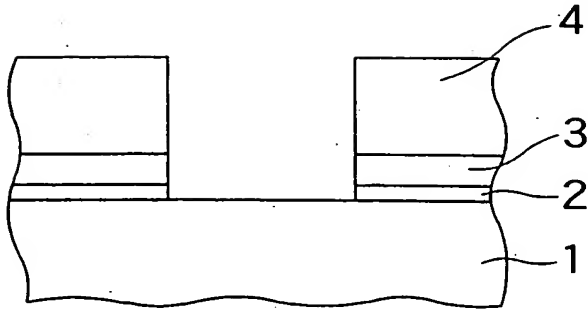


FIG. 2A

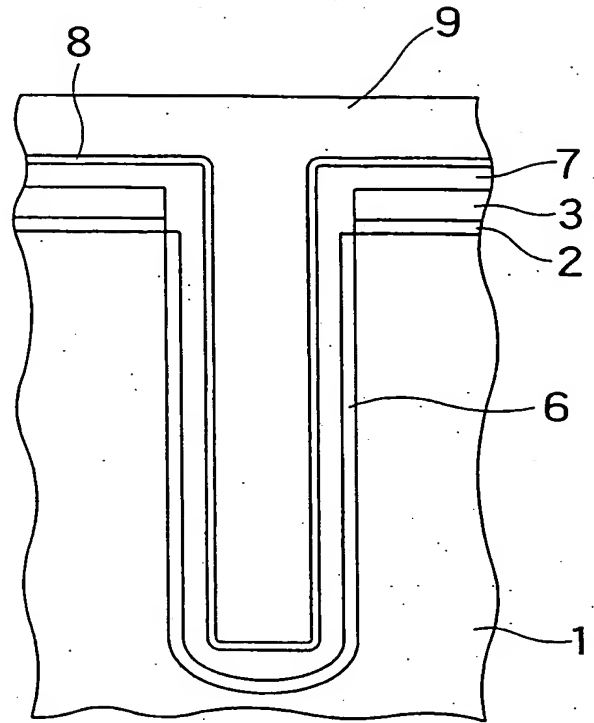


FIG. 2C

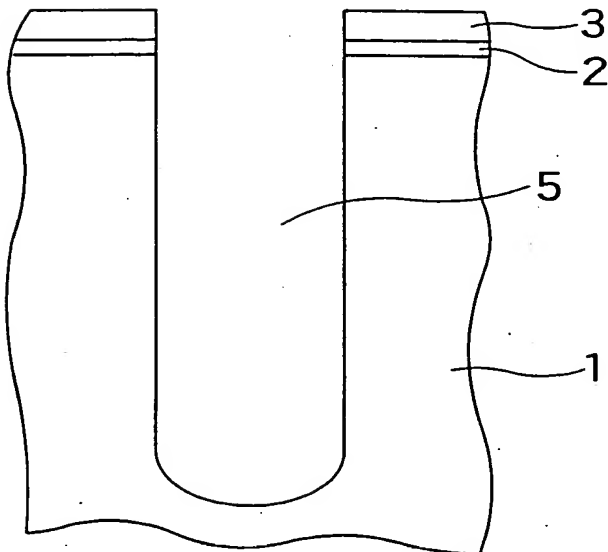


FIG. 2B

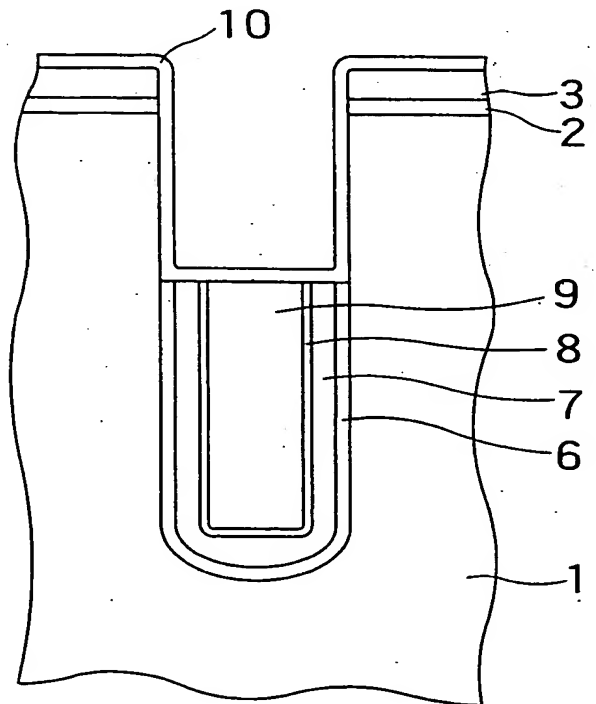


FIG. 2D

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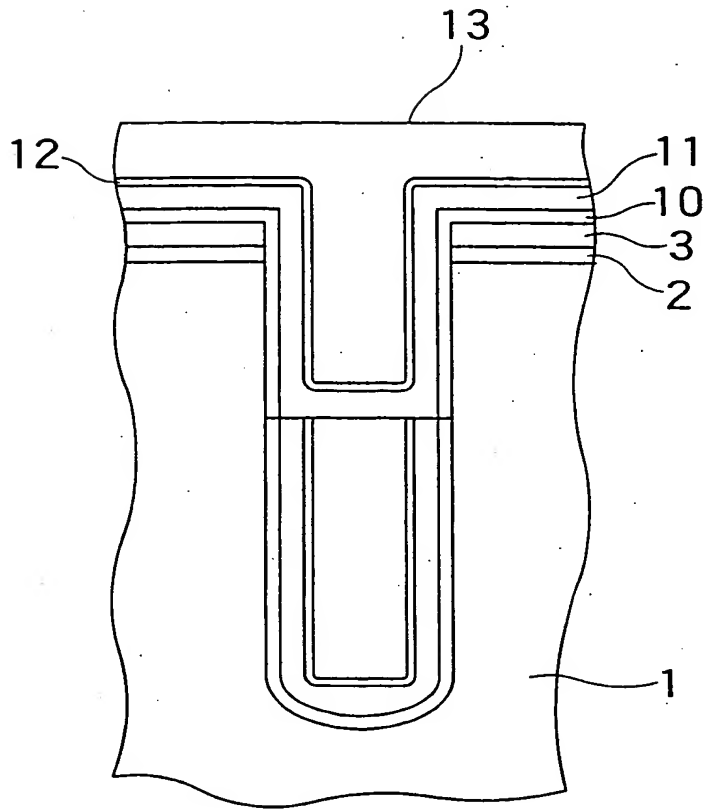


FIG. 3A

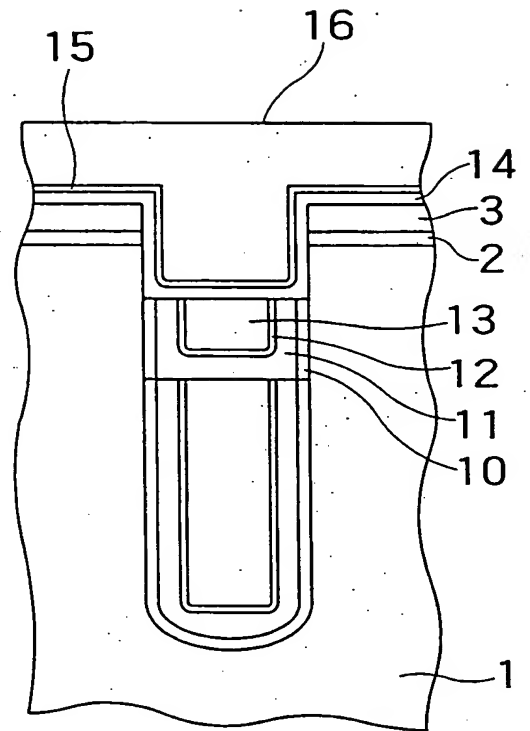


FIG. 3B

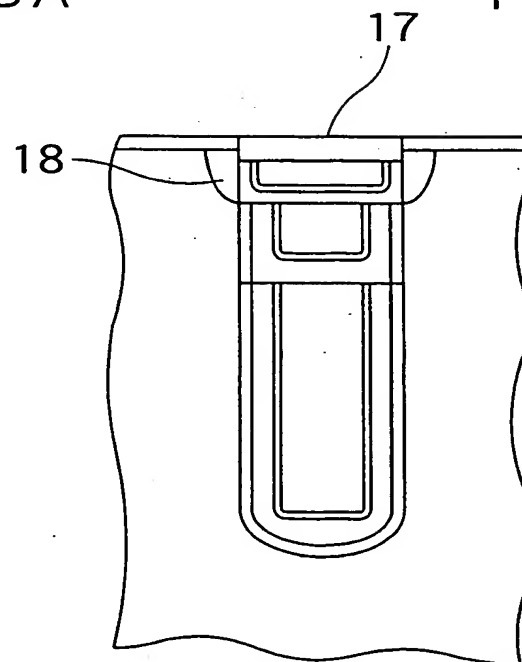


FIG. 3C



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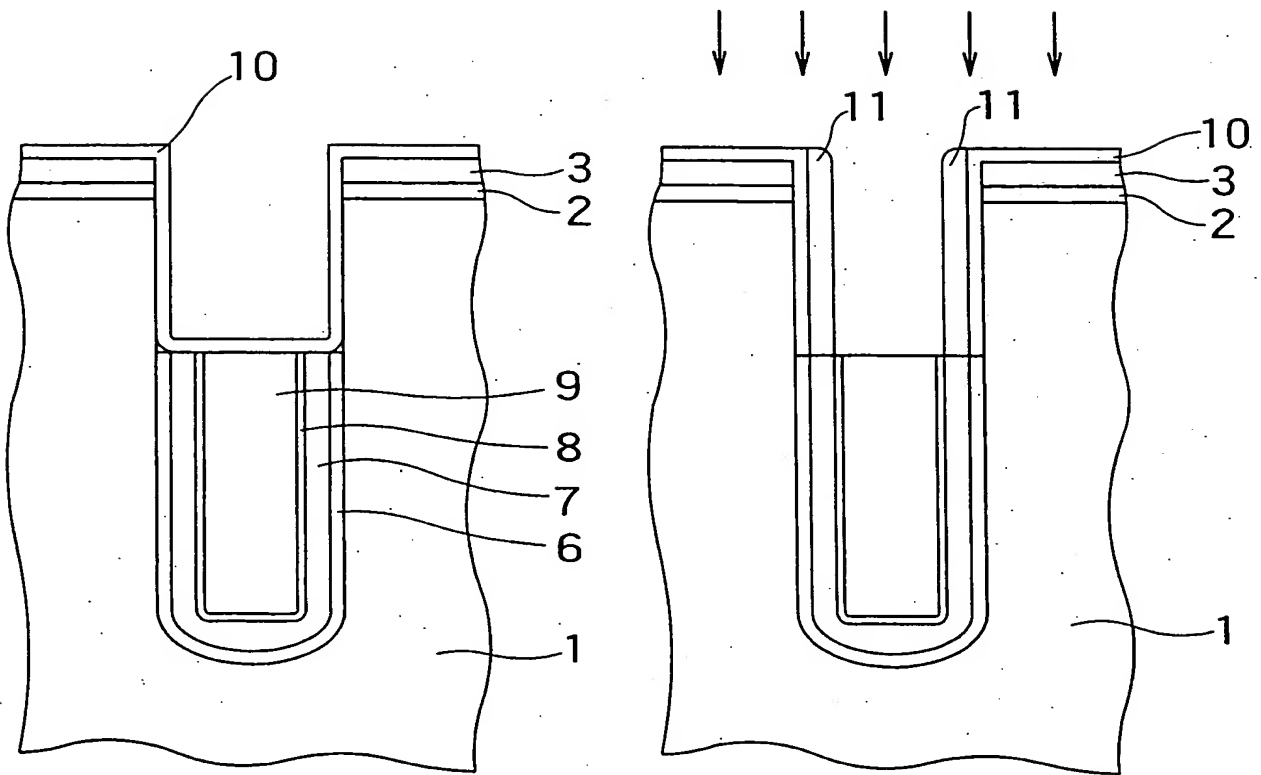


FIG. 5A

FIG. 5B

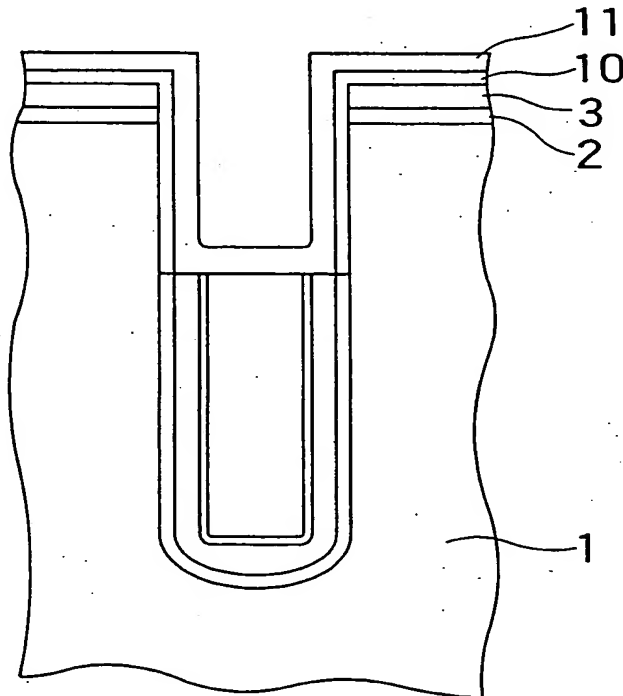


FIG. 5C

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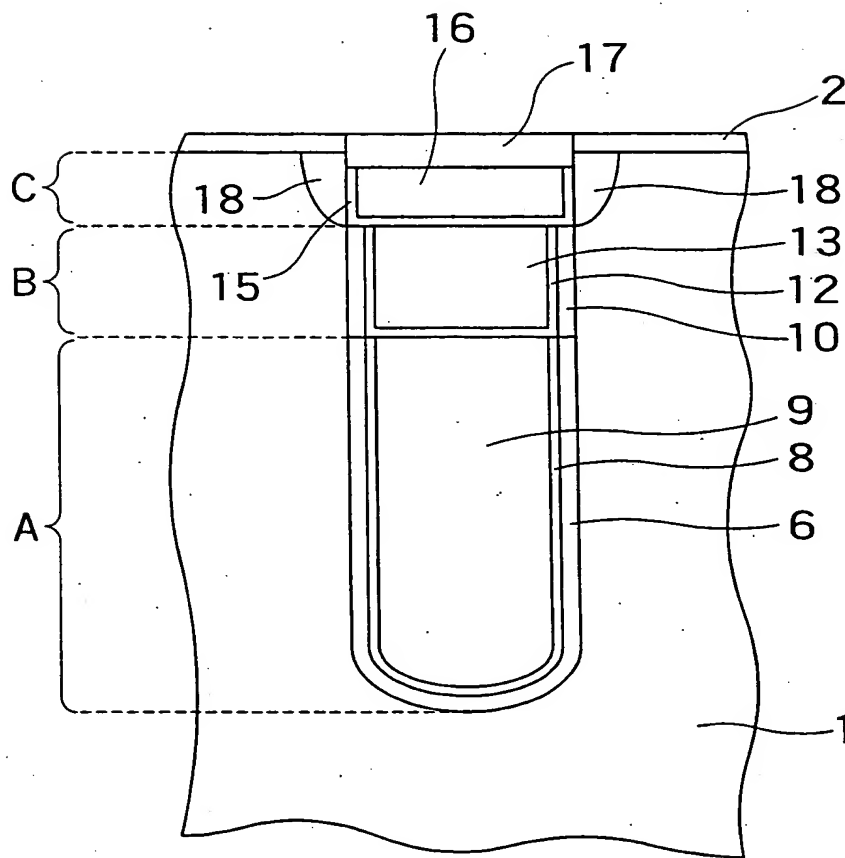
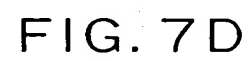
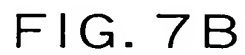
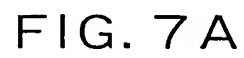


FIG. 6



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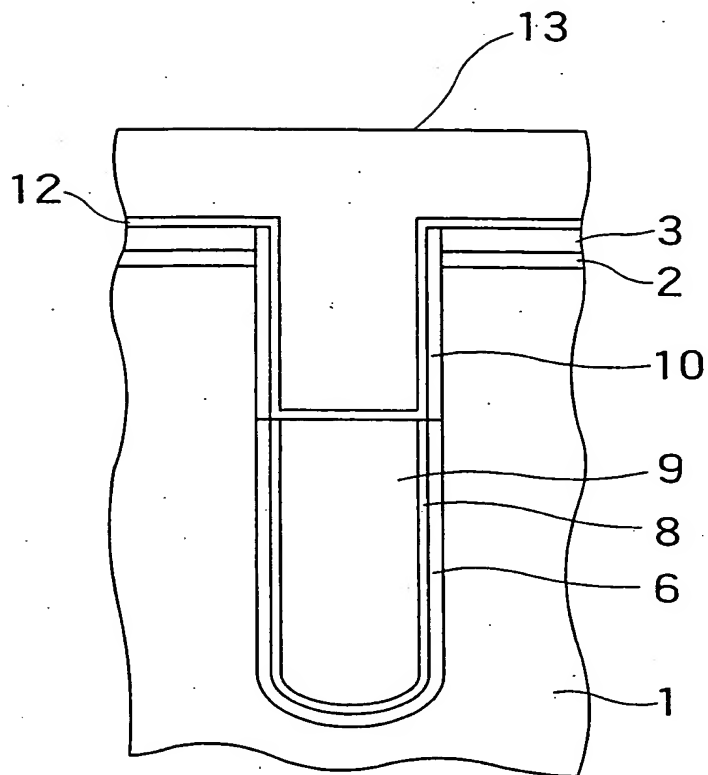


FIG. 8A

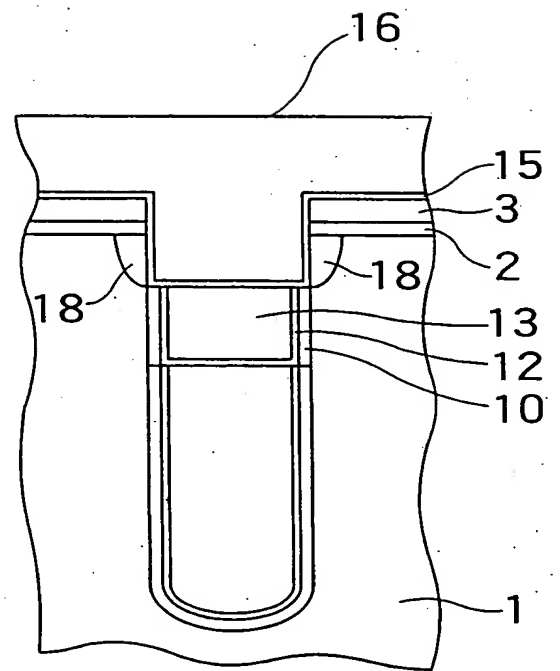


FIG. 8B

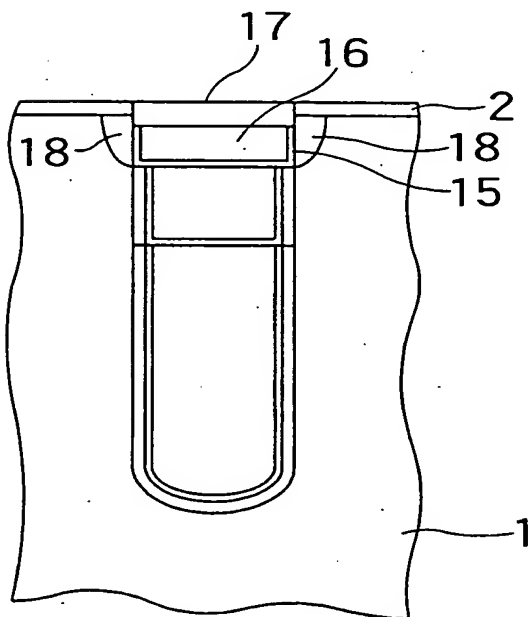


FIG. 8C



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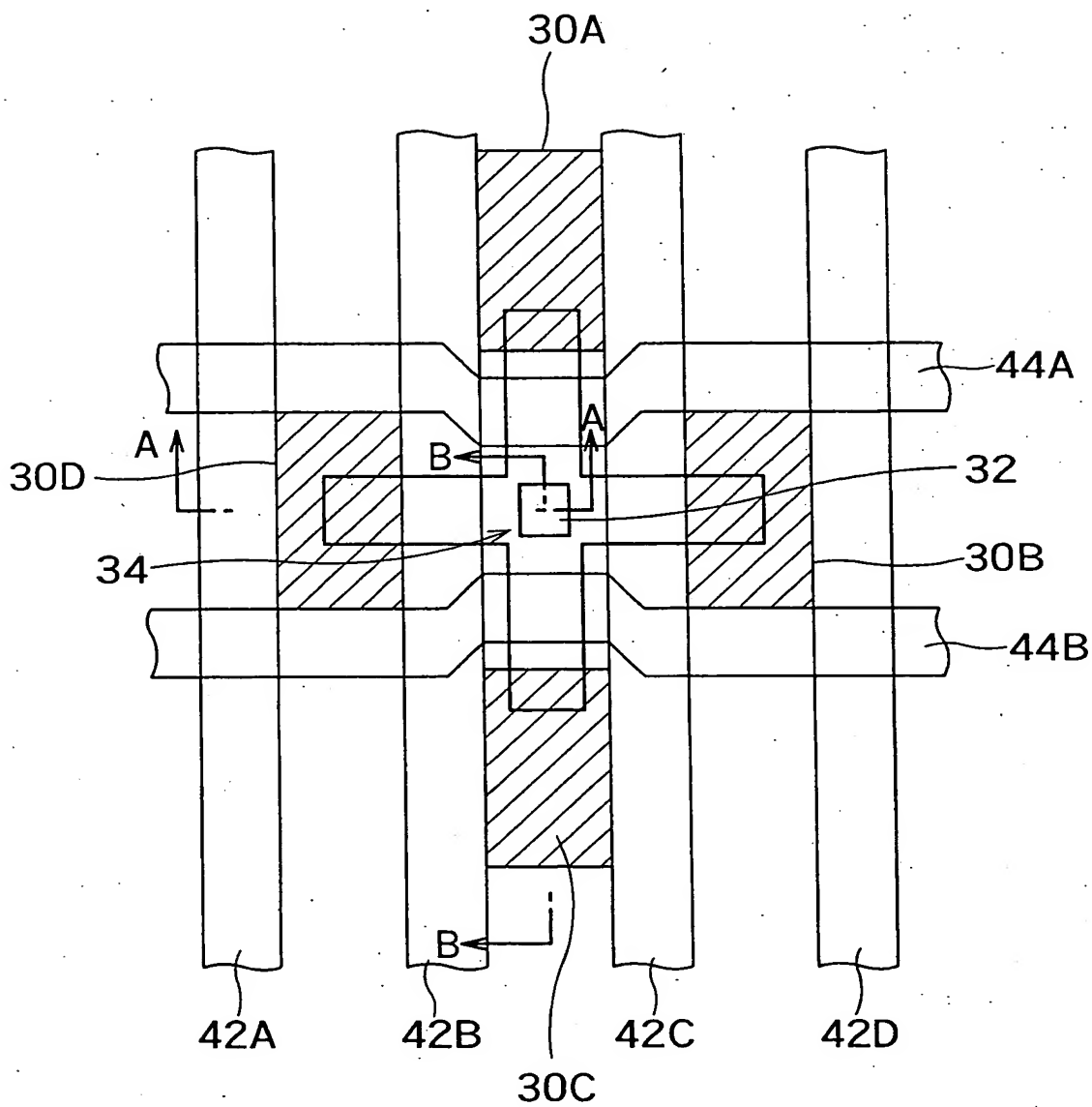


FIG. 9

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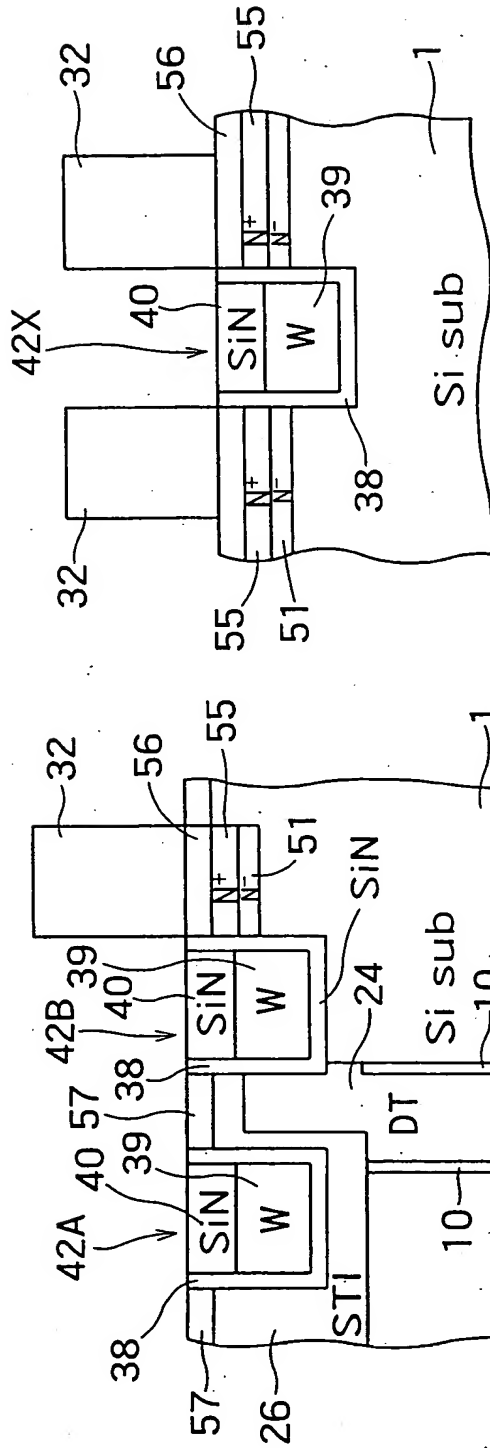


FIG. 10C

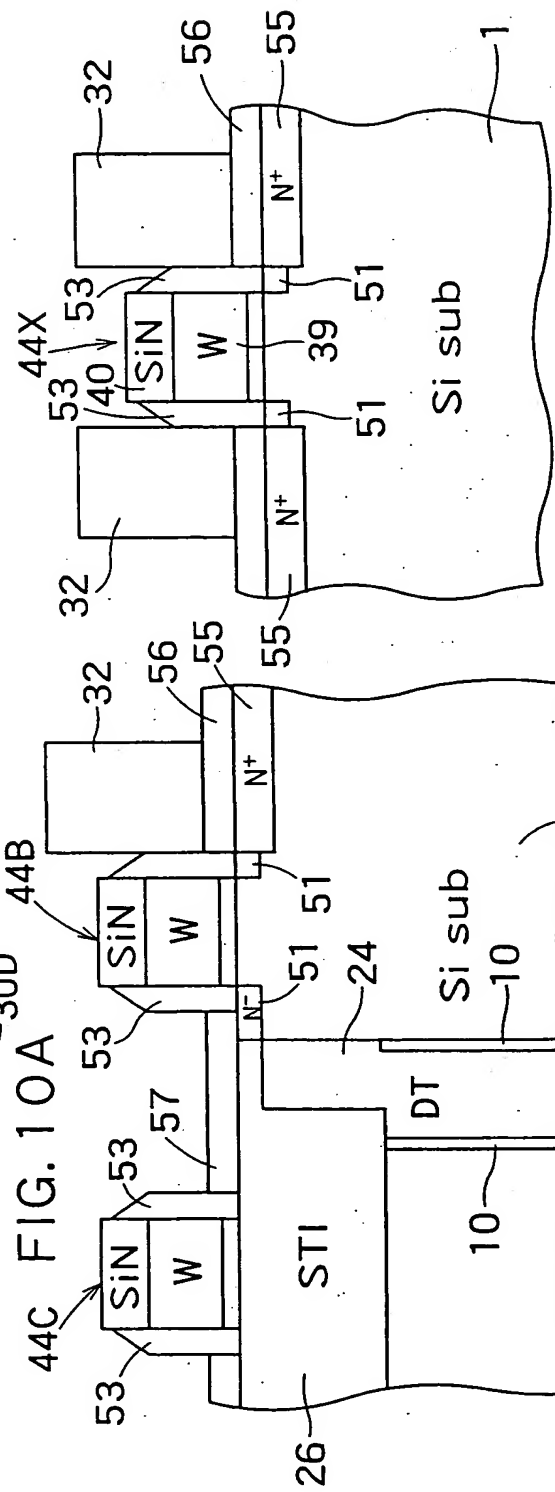


FIG. 10D

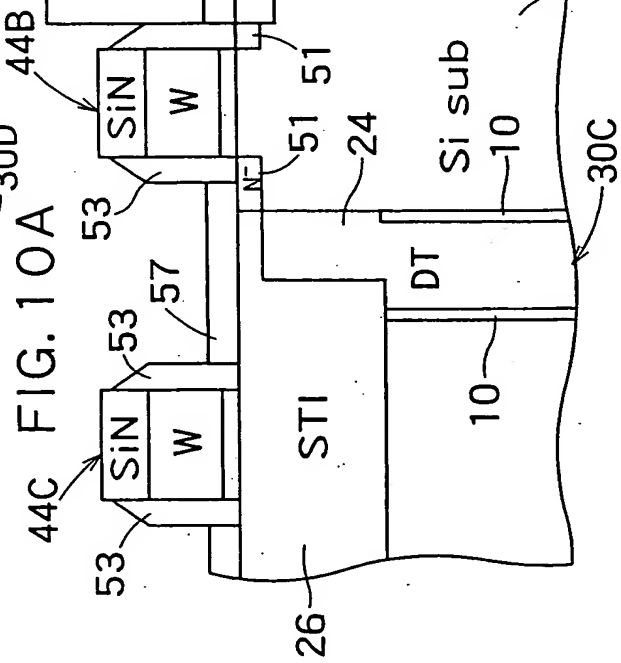


FIG. 10A

FIG. 10B

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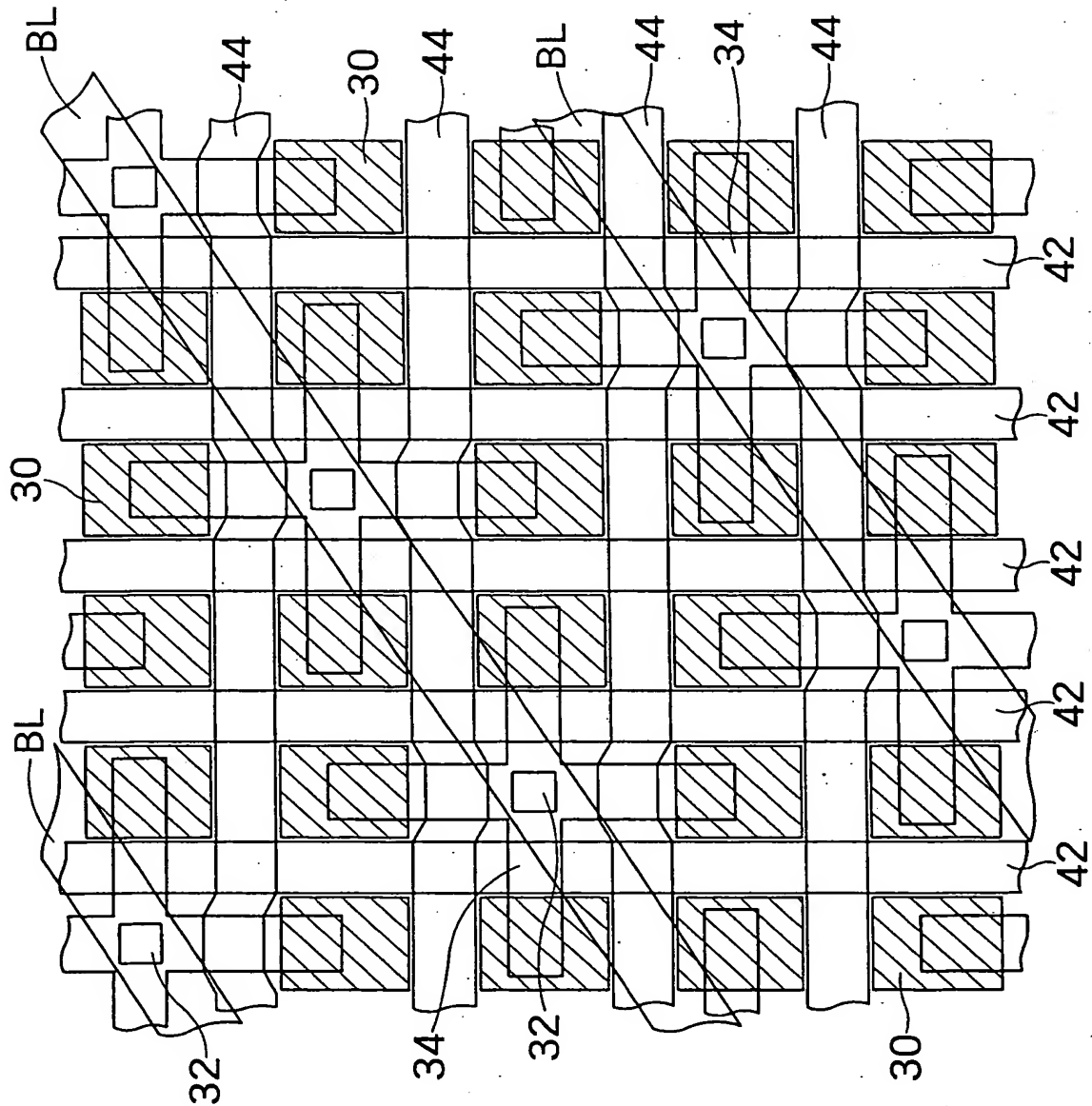


FIG. 11

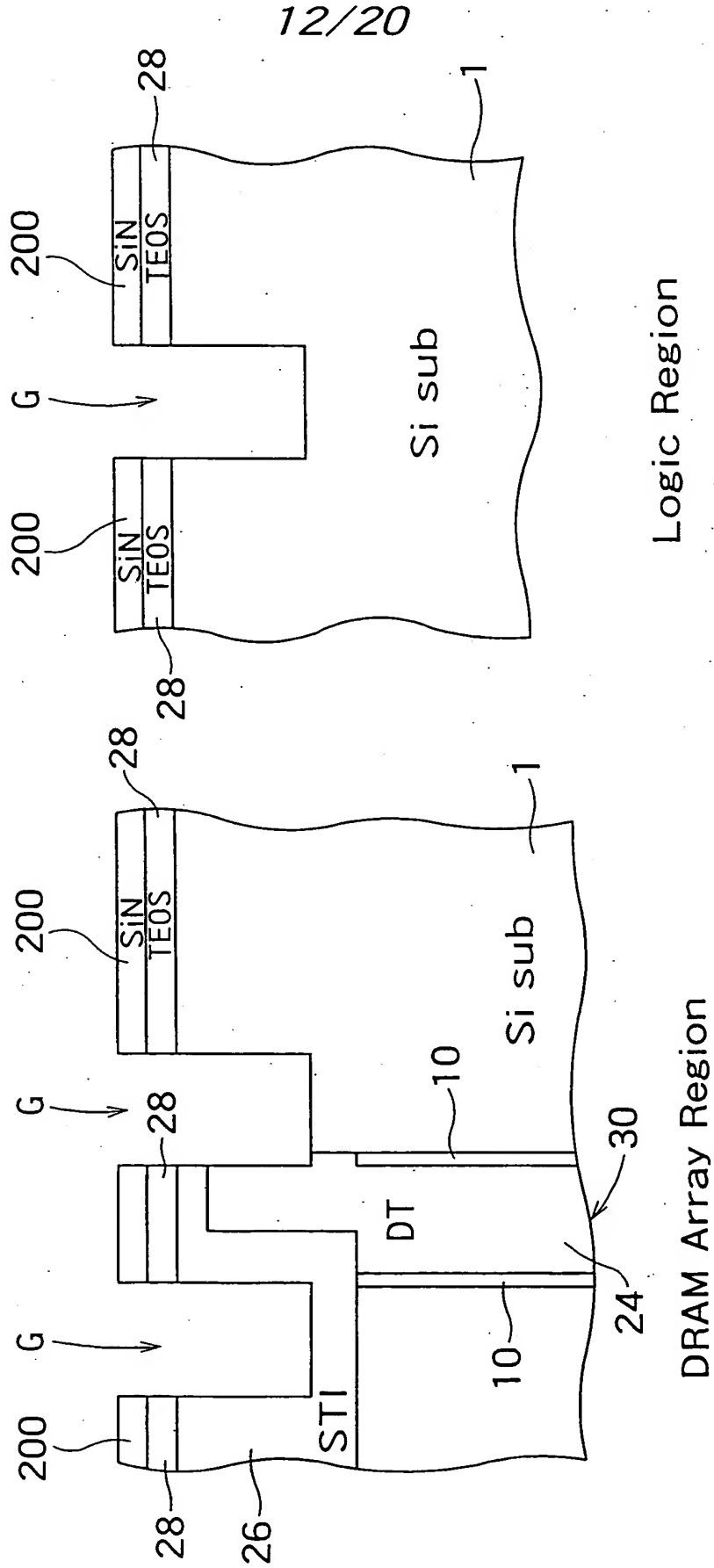
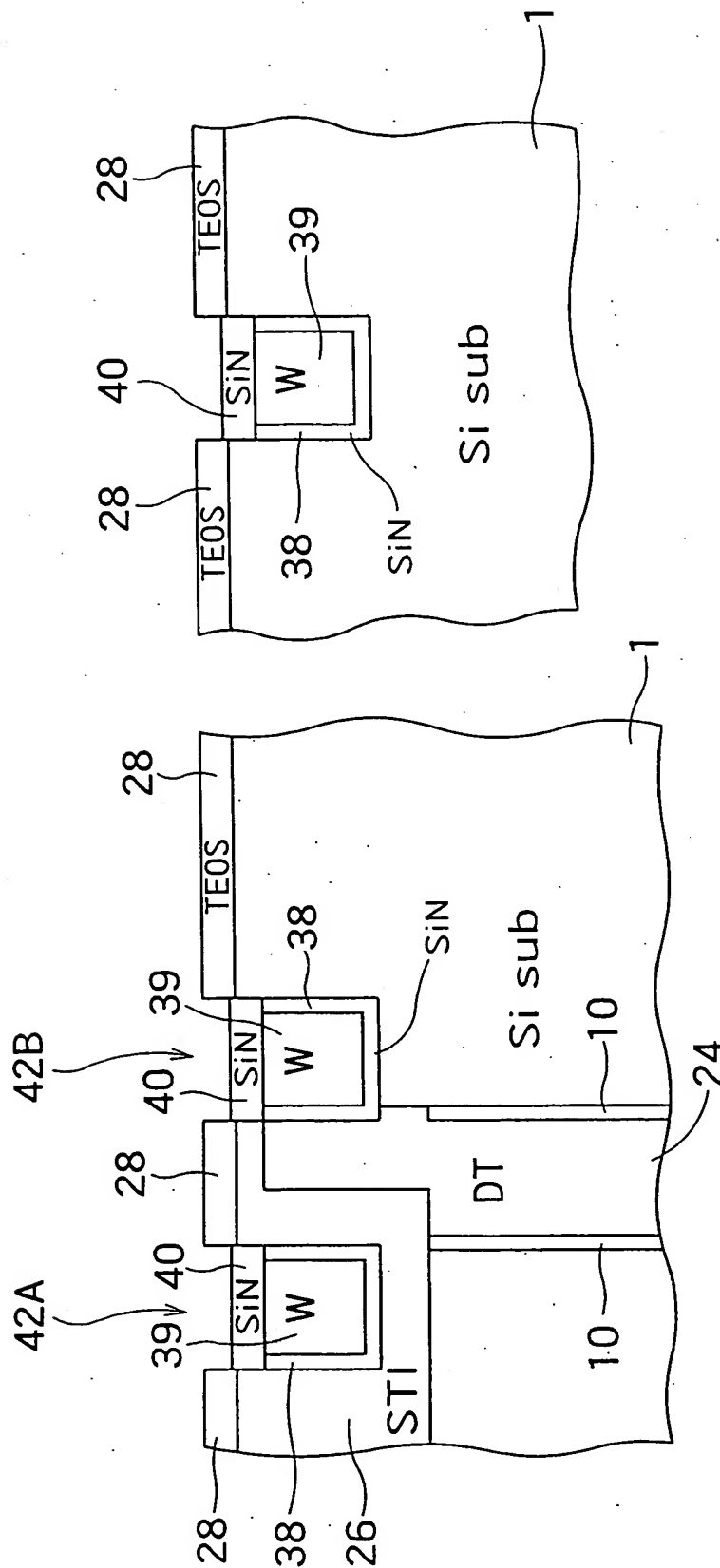


FIG. 12B

FIG. 12A

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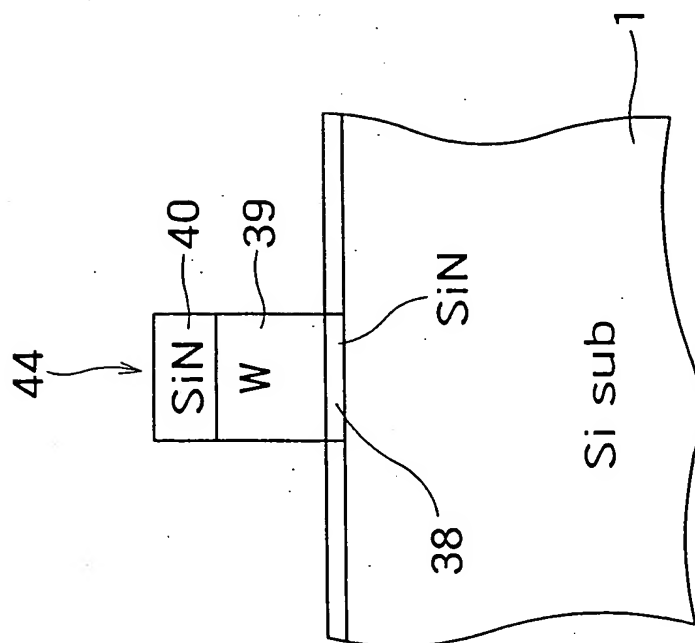
Logic Region

FIG. 13B

DRAM Array Region

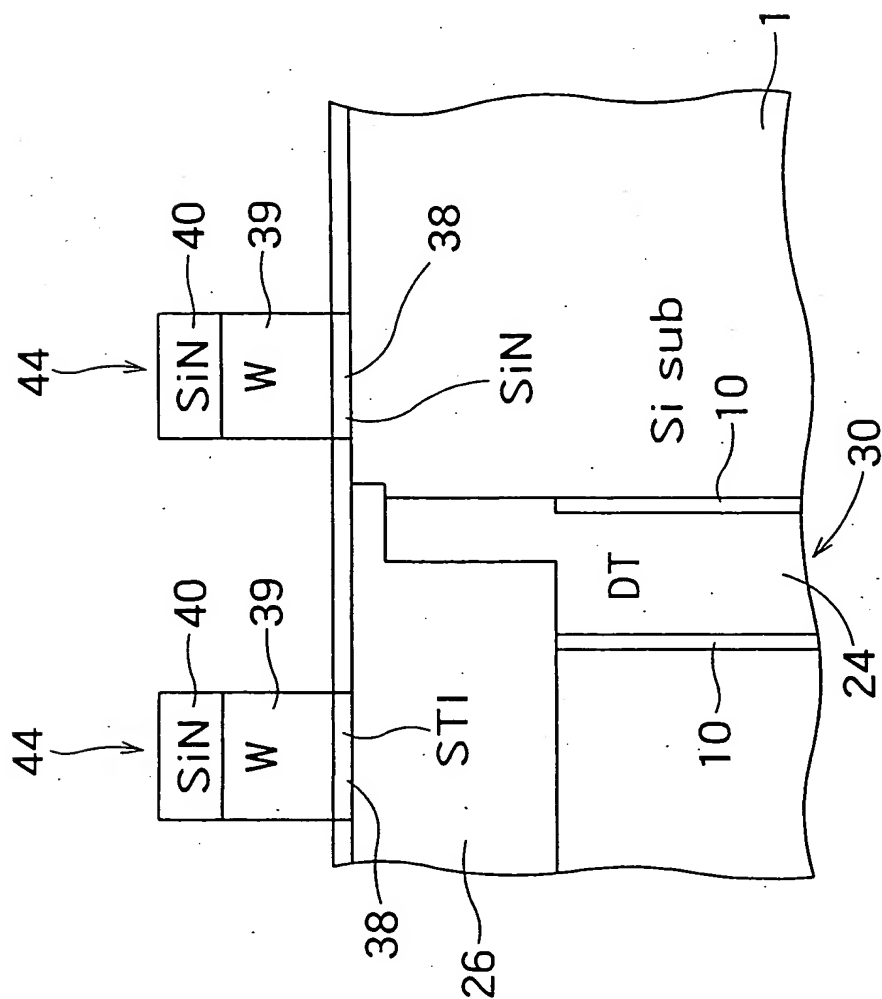
FIG. 13A

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Logic Region

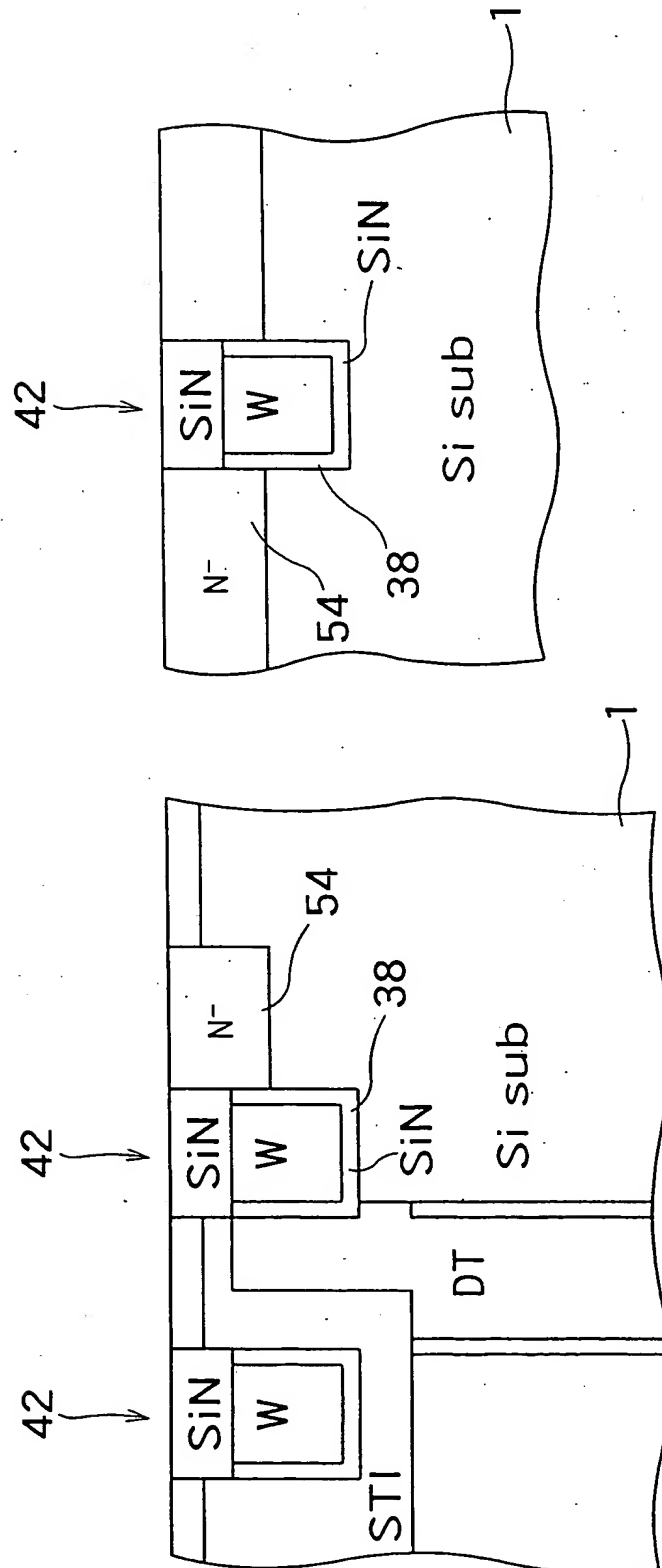
FIG. 14B



DRAM Array Region

FIG. 14A

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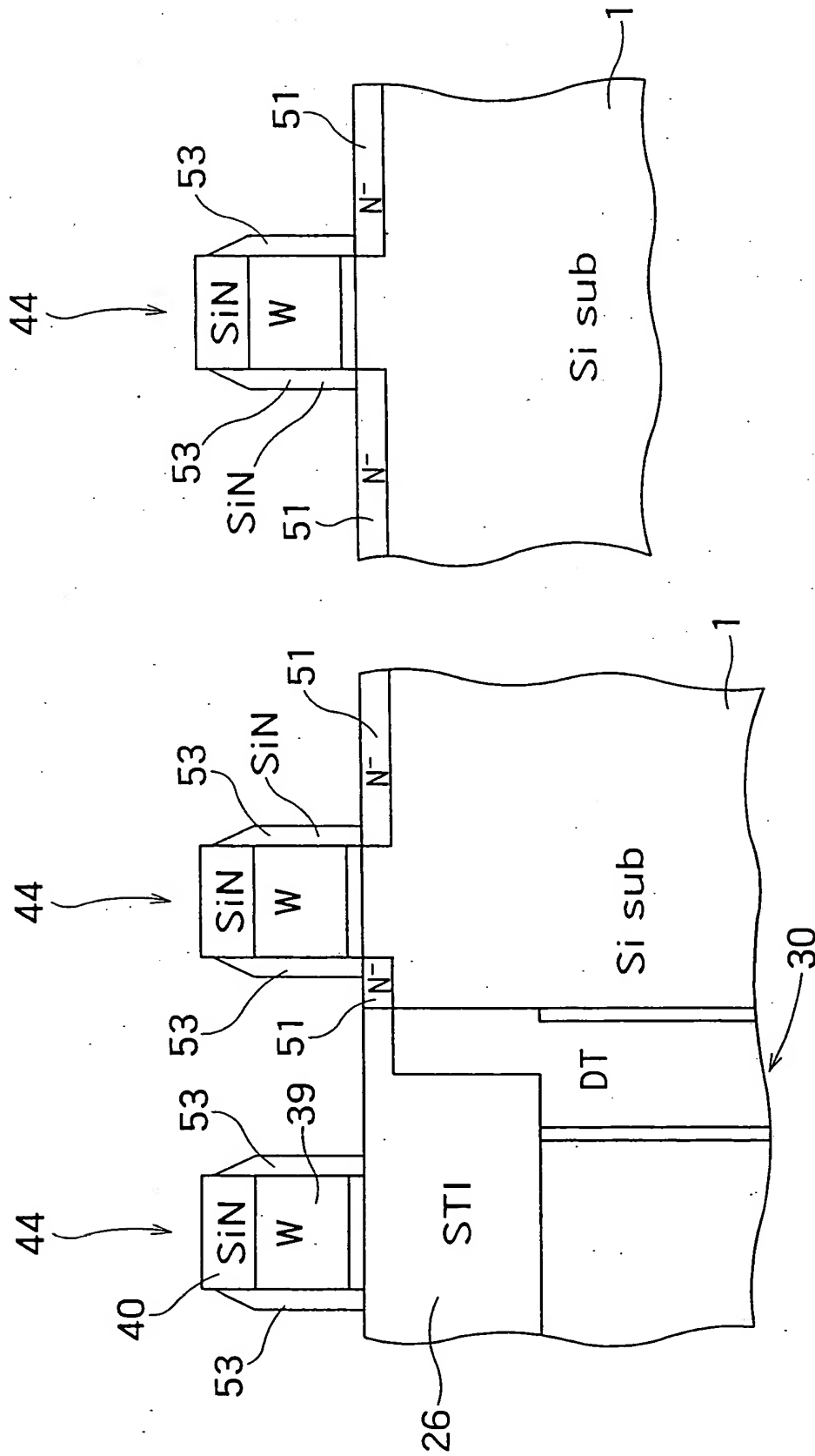
## Logic Region

FIG. 15B

## DRAM Array Region

FIG. 15A

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Logic Region

FIG. 16B

DRAM Array Region

FIG. 16A





FIG. 17B

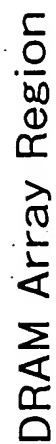
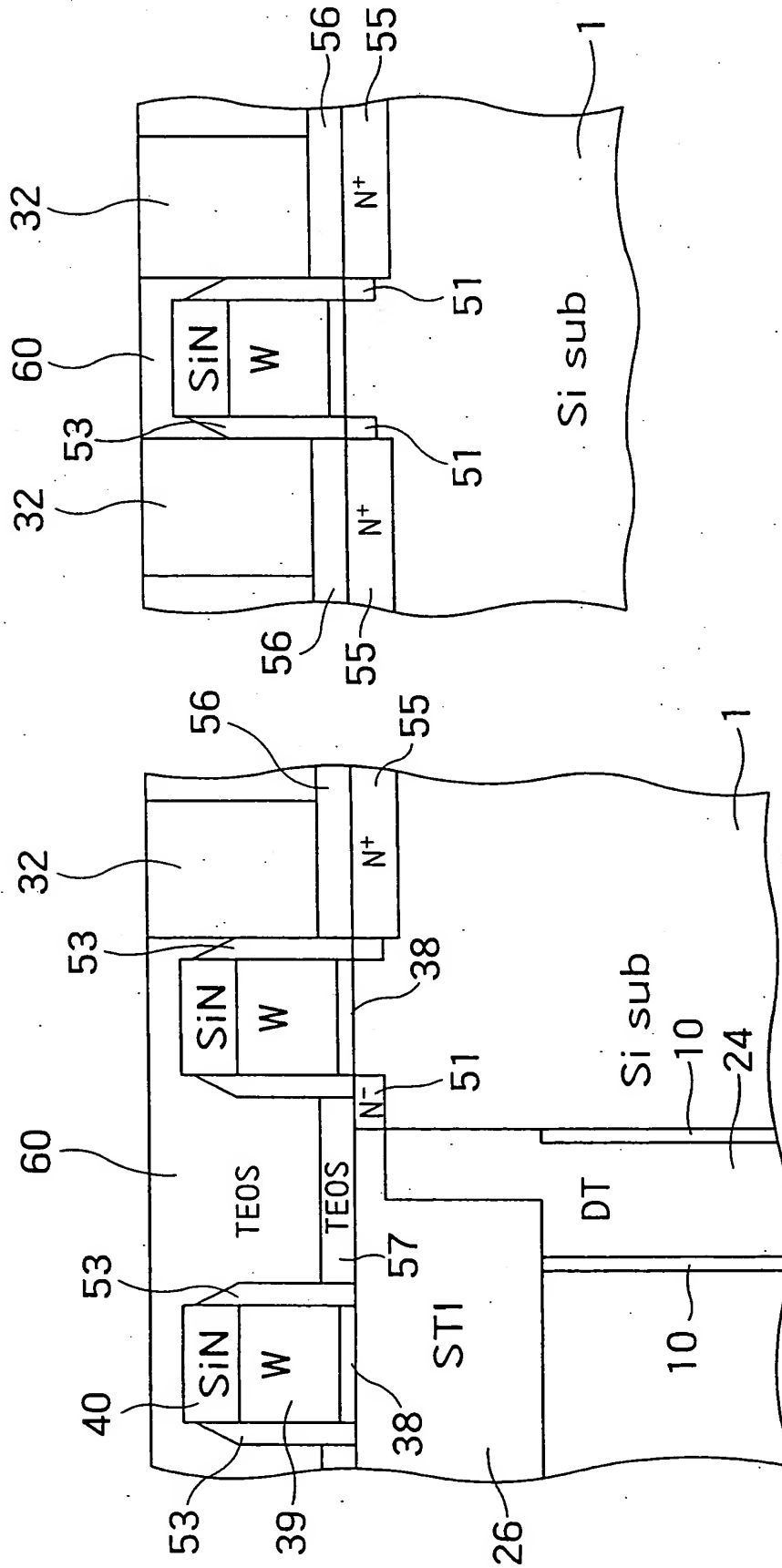


FIG. 17A

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Logic Region

FIG. 18B

DRAM Array Region

FIG. 18A

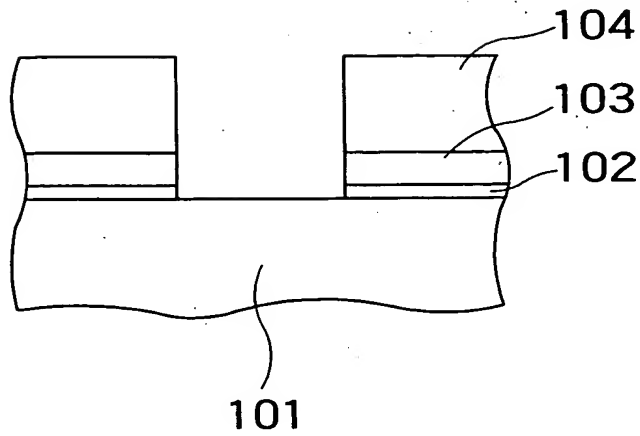


FIG. 19A  
(PRIOR ART)

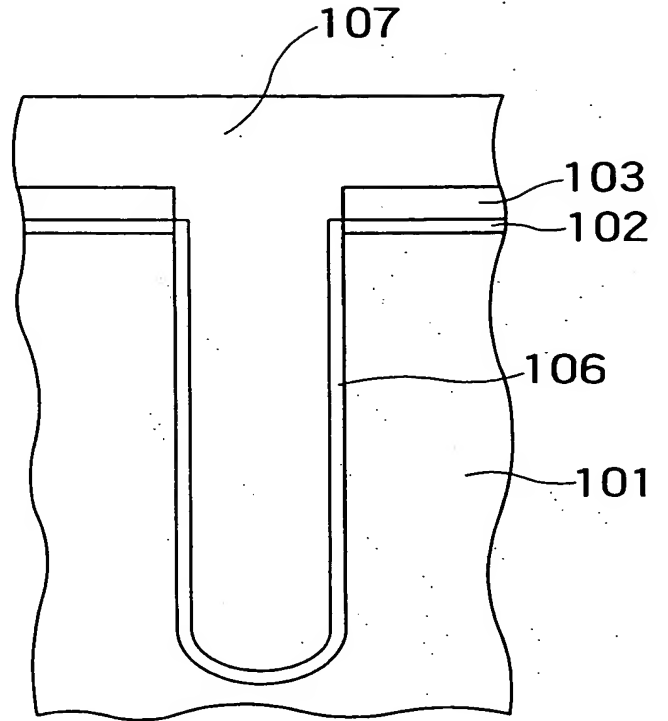


FIG. 19C  
(PRIOR ART)

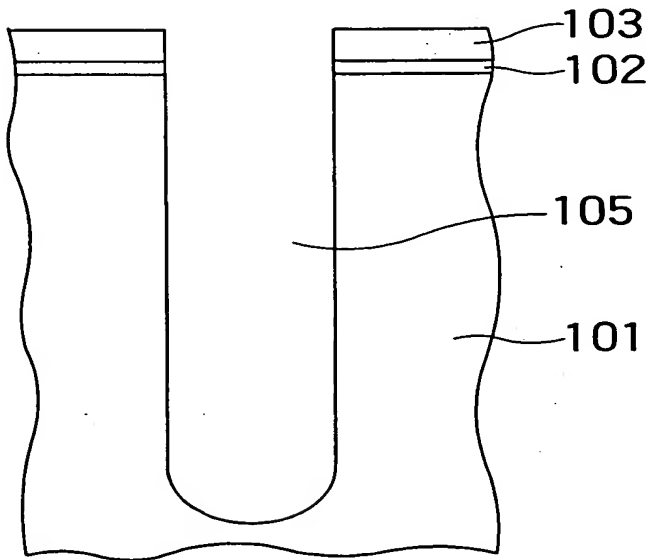


FIG. 19B  
(PRIOR ART)

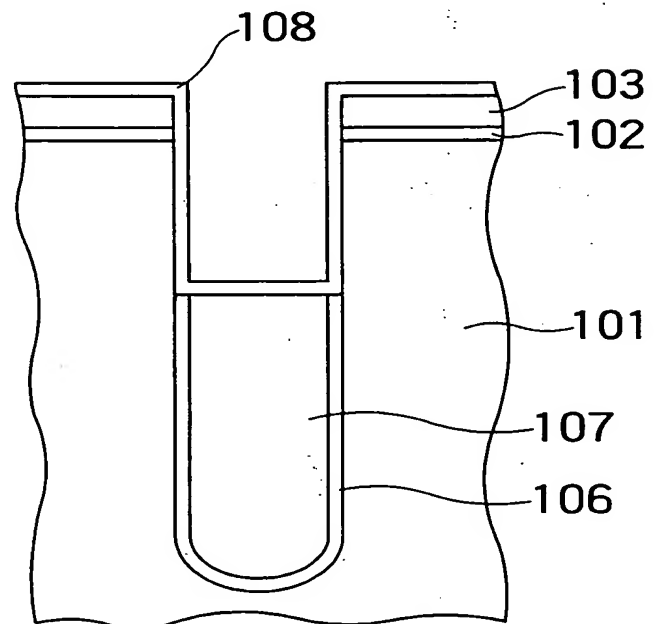


FIG. 19D  
(PRIOR ART)

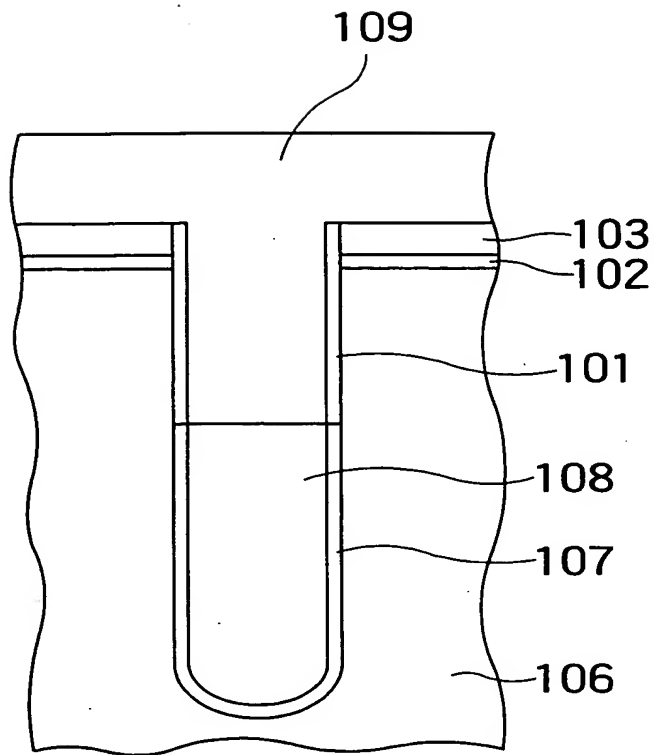


FIG. 20A  
(PRIOR ART)

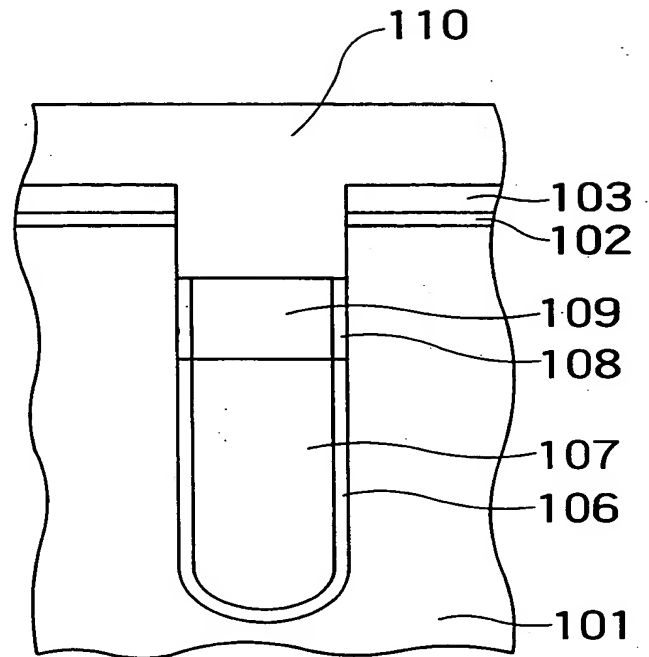


FIG. 20B  
(PRIOR ART)

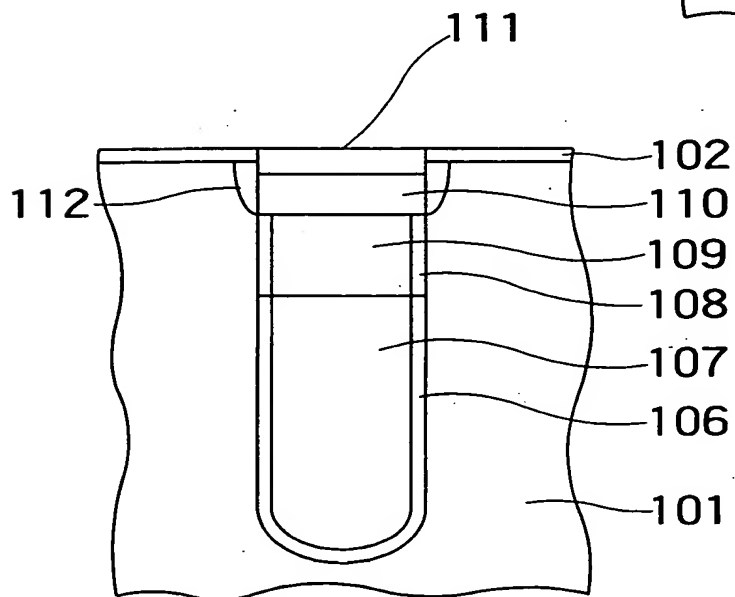


FIG. 20C  
(PRIOR ART)